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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,762	10/15/2003	Shiv Kumar Gupta	15164US01	6313

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EXAMINER	
GEBRESILASSIE, KIBROM K	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 05/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/685,762	GUPTA, SHIV KUMAR	
	Examiner	Art Unit	
	Kibrom K. Gebresilassie	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the amended application filed on October 15, 2003.

2. Claims 1-11 have been examined and rejected.

Oath/Declaration

3. The Office acknowledges receipt of properly signed oath/declaration filed October 15, 2003.

Drawings

4. The drawings are objected to because they are too dark to read (Fig. 1A, Fig. 1B, Fig. 2, and Fig. 4). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

5. Figures 1A and 1B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

6. Claim 11 is objected to because of the following informalities: in claim 11 the word emulator is not mentioned. It is therefore difficult if claim 11 has an interconnection with the rest of the claims. Appropriate correction is required.

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 6, 10, and 11 are rejected under 35 U.S.C. 101 because the claimed invention is drawn to non-statutory subject matter.

Per independent claims 6, 10, and 11: The Examiner first submits that, in view of the language of the claims, method claim 6 is abstract and does not appear to recite a tangible result. In this case the result appears to merely be an abstract set of system elements that are not used to achieve the application recited in the preamble of the claim. The examiner submits that in order to establish a practical application, there

must be either a physical transformation, or a useful, concrete and tangible result. Data transformation is not the same as a physical transformation. In this instance, there does not appear to be a tangible result. Here, the recited system elements simply result in an un-stored and un-applied "connection" , and not a physical transformation. The claimed elements in this case, are simply a thought or computation element, and not in and of themselves a tangible result. It is not until the transformation of the elements is applied in a meaningful way that it has real world value and becomes a tangible result.

MPEP 2106 recites the following:

"A. Identify and Understand Any Practical Application Asserted for the Invention
The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and ***tangible result****." State Street, 149 F.3d at 1373, 47 USPQ2d at 1601-02. The purpose of this requirement is to limit patent protection to inventions that possess a certain level of* ***"real world" value****, as opposed to subject matter that represents nothing more than an idea or concept, or is simply a starting point for future investigation or research (Brenner v. Manson, 383 U.S. 519, 528-36, 148 USPQ 689, 693-96); In re Ziegler, 992, F.2d 1197, 1200-03, 26 USPQ2d 1600, 1603-06 (Fed. Cir. 1993)). Accordingly, a complete disclosure should contain some indication of the practical application for the claimed invention, i.e., why the applicant believes the claimed invention is useful.*
Apart from the utility requirement of 35 U.S.C. 101, usefulness under the patent eligibility standard requires significant functionality to be present to satisfy the useful result aspect of the practical application requirement. See Arrhythmia, 958 F.2d at 1057, 22 USPQ2d at 1036. Merely claiming nonfunctional descriptive material stored in a computer-readable medium does not make the invention eligible for patenting. For example, a claim directed to a word processing file stored on a disk may satisfy the utility requirement of 35 U.S.C. 101 since the information stored may have some "real world" value. However, the mere fact that the claim may satisfy the utility requirement of 35 U.S.C. 101 does not mean that a useful result is achieved under the practical application requirement. The claimed invention as a whole must produce a "useful, concrete and tangible" result to have a practical application.
Although the courts have yet to define the terms useful, concrete, and tangible in the context of the practical application requirement for purposes of these guidelines, the following examples illustrate claimed inventions that have a practical application because they produce useful, concrete, and tangible result:
- Claims drawn to a long-distance telephone billing process containing mathematical algorithms were held to be directed to patentable subject matter because "the claimed process applies the Boolean principle to produce a useful, concrete, ***tangible result*** *without pre-empting other uses of the mathematical principle." AT &T Corp. v. Excel Communications, Inc., 172 F.3d 1352, 1358, 50 USPQ2d 1447, 1452 (Fed. Cir. 1999);*
- "[T]ransformation of data, representing discrete dollar amounts, by a machine through a series of mathematical calculations into a final share price, constitutes a practical

application of a mathematical algorithm, formula, or calculation, because it produces a useful, concrete and tangible result' -- a final share price momentarily fixed for recording and reporting purposes and even accepted and relied upon by regulatory authorities and in subsequent trades." State Street, 149 F.3d at 1373, 47 USPQ2d at 1601; and
- Claims drawn to a rasterizer for converting discrete waveform data samples into anti-aliased pixel illumination intensity data to be displayed on a display means were held to be directed to patentable subject matter since the claims defined "a specific machine to produce a useful, concrete, and ***tangible result****." In re Alappat, 33 F.3d 1526, 1544, 31 USPQ2d 1545, 1557 (Fed. Cir. 1994)."*

Dependent claims 7-9 inherit the defects of the claims from which they depend.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-7, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,572,710 issued to Asano et al.

As per Claim 1:

Asano discloses a hardware emulator for verifying a plurality of systems on chip, said emulator comprising: a first circuitry for verifying a first system on chip; and a second circuitry for verifying a second system on chip while verifying the first system on chip (col. 7 lines 55-63; Fig. 2).

As per Claim 2:

Asano discloses the hardware emulator of claim 1, further comprising: a first interface for providing inputs to the first circuitry and receiving outputs from the first circuitry; and a second interface for providing inputs to the second circuitry and receiving outputs from the second circuitry (col. 7 lines 64-67 and continue to col. 8

lines 1-4; Fig. 2 element 2).

As per Claim 3:

Asano discloses the hardware emulator of claim 1, wherein the first circuitry is configured to realize the first system on chip (col. 8 lines12-27) and the second circuitry is configured to realize the second system on chip (col. 7 lines 53-64).

As per Claim 4:

Asano discloses a hardware emulator for verifying a plurality of systems on chip, said emulator comprising: a first circuitry configured to realize a first system on chip (col. 8 lines12-27); and a second circuitry configured to realize a second system on chip (col. 7 lines 53-64) while verifying the first system on chip, the second circuitry connected to the first circuitry (col. 7 lines 58-60).

As per Claim 5:

Asano discloses the hardware emulator of claim 4, further comprising: a first interface operably connected to the first circuitry, wherein the first interface provides inputs to the first circuitry and receives outputs from the first circuitry; and a second interface operably connected to the second circuitry, wherein the second interface provides inputs to the second circuitry and receives outputs from the second circuitry (col. 7 lines 64-67 and continue to col. 8 lines 1-4; Fig. 2 element 2).

As per Claim 6:

Asano discloses a method for verifying a plurality of systems on chip, the method comprising: verifying a first system on chip with a first portion of a hardware emulator; and verifying a second system on chip with a second portion of the hardware emulator

while verifying the first system on chip (col. 7 lines 55-63; Fig. 2).

As per Claim 7:

Asano discloses the method of claim 6, further comprising: configuring the first portion of the hardware emulator to realize the first system on chip (col. 8 lines12-27); and configuring the second portion of the hardware emulator to realize the second system on chip (col. 7 lines 53-64).

As per Claim 9:

Asano discloses the method of claim 6, wherein verifying the first system on chip further comprises: providing inputs to the first portion; and receiving outputs from the first portion (col. 7 lines 64-67 and continue to col. 8 lines 1-4).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 8, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,572,710 issued to Asano et al, in view of Kerr et al.

As per Claim 8:

Asano discloses the method of claim 7, wherein configuring the first portion of the hardware emulator comprises receiving a portion of a describing the first system on chip and wherein configuring the second portion of the hardware emulator comprises receiving another portion of a top wrapper describing the second system on chip (col. 7 lines 55-63; Fig. 2).

Asano fails to disclose a top wrapper.

Kerr discloses a top wrapper (Abstract).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Asano related to a logic simulation system to be used for a simulation of logic circuits in designing and verification of a digital system using logic circuits with the teachings of Kerr related to improve integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers. The motivation for doing so would have been more convenient to access the entire memory space in the system, including the entire virtual memory space accessible by host processor (col. 3 lines 49-53). Hence a skilled artisan having access to the teaching of Asano and Kerr would have knowingly modified the teaching of Asano with Kerr.

As per Claim 10:

The limitation of claim 10 has already been discussed in the rejection of Claim 8. It is therefore rejected under the same rationale.

As per Claim 11:

Asano discloses a computer readable medium storing a data structure, the data structure (Fig. 38 and 39) comprising: a first design structure for describing a first system on chip (col. 8 lines12-27), wherein the first design structure further comprises: declaration for describing ports associated with the first system on chip (Abstract lines 7-13); a first design information for describing at least a portion of the first system on chip (col. 8 lines12-27); and an end of first design structure indicator, for indicating the end of the first design structure; and a second design structure for describing the second system on chip (col. 10 lines 22-28), wherein the second design structure further comprises: declaration for describing ports associated with the second system on chip (Abstract lines 7-13); a second design information for describing at least a portion of the first system on chip (col. 7 lines 53-64); and an end of second design structure indicator, for indicating the end of the second design indicator; and the second design structure immediately following the end of first design structure indicator (col. 7 lines 15-25).

Asano fails to disclose first and second ports.

Kerr discloses first and second ports (Abstract).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Asano related to a logic simulation system to be used for a simulation of logic circuits in designing and verification of a

digital system using logic circuits with the teachings of Kerr related to improve integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers. The motivation for doing so would have been more convenient to access the entire memory space in the system, including the entire virtual memory space accessible by host processor (col. 3 lines 49-53). Hence a skilled artisan having access to the teaching of Asano and Kerr would have knowingly modified the teaching of Asano with Kerr.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Publication No. 2003/0212539 A1 issued to Beausoleil et al.

2. Any inquiring concerning this communication or earlier communication from the examiner should be directed to Kibrom K. Gebresilassie whose telephone number is (571) 272-8571. The examiner can normally be reached on Monday-Friday, 8:30 am to 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Kamini shah can be reached at (571) 272-2279. The official fax number is (571) 273-8300. Any inquiring of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is (571) 272-3700.

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